PROJECT WORKFLOW

TEAM : CF-RV-25-14

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PROBLEM STATEMENT: C-Class core/trace/log RTL implementation, simulation and FPGA: Add support to send and read the PC (or more data like instruction, register values) from instruction commit log (rtl.dump). Phase1:Test on coremark with gdb in simulation and FPGA.

PLAN DESCRIPTION:

* To analyse and understand the RTL file of write back stage which is the stage5 of src in [shakti / cores / c-class · GitLab](https://gitlab.com/shaktiproject/cores/c-class) where we can access PC, instructions and register writeback values .
* To modify the file by adding the logic to extract the necessary signals.
* Simulation of the modified RTL is to be done in Verilator by which rtl.dump and coremark.elf files can be generated after coremark execution.
* To load the files to FPGA and debug using GDB.
* To observe their register files and compare with the extracted dump file.