CF-RV-25-14

PROJECT WORKFLOW

PHASE 1

We planned to analyse and understand the RTL file of write back stage which is the stage5 of src in [shakti / cores / c-class · GitLab](https://gitlab.com/shaktiproject/cores/c-class) where we can access PC, instructions and register writeback values . Then, we are yet to modify the file by adding the logic to extract the necessary signals. Then, simulation of the modified RTL is done in Verilator by which rtl.dump and coremark.elf files can be generated after coremark execution. They are then loaded to FPGA and debugged using GDB. Their register states are observed and compared with the extracted dump file.